IN THE CLAIMS:

The text of all pending claims (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 2, 6, 7 and 11 in accordance with the following:

1. (PREVIOUSLY PRESENTED) A clock regeneration circuit, comprising:

a PLL circuit which includes a voltage control oscillator, for synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of a reception signal;

a clock extraction circuit which includes a band passing filter having a passing band width which concurrently extracts a basic waves component of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception signal;

a frequency detector for detecting a difference in frequencies between an output of the clock extraction circuit and an oscillation frequency of the voltage control oscillator;

a filter for controlling the oscillation frequency of the voltage control oscillator of the PLL circuit at a detection output of the frequency detector;

a bit rate detection circuit for detecting a bit rate of the reception signal; and

a frequency selection circuit for outputting the oscillation frequency of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to the bit rate detected by the bit rate detection circuit, as a regeneration clock signal.

2. (CURRENTLY AMENDED) The clock regeneration circuit according to claim 1, wherein

the clock extraction circuit further includes:

a delay circuit for delaying the reception signal by a half cycle of the reception signal; and

an EX-OR circuit for acquiring an exclusive OR operation of an output of the delay circuit and the reception signal, wherein

the output of the EX-OR circuit is coupled to the band passing filter ~~in the configuration~~.

3. (PREVIOUSLY PRESENTED) The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

a first AND gate for taking a conjunction of the reception signal and the oscillation frequency signal of the voltage control oscillator of the PLL circuit;

a delay circuit for delaying an output of the first AND gate by 1 cycle of the oscillation frequency signal of the voltage control oscillator;

a second AND gate for taking a conjunction of an output of the first AND gate and an output of the delay circuit; and

a circuit for acquiring an average value of the output of the second AND gate.

4. (PREVIOUSLY PRESENTED) The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

an OR gate for synthesizing the reception signal with a signal obtained by inverting the reception signal; and

a circuit for acquiring an average value of the output of the OR gate.

5. (PREVIOUSLY PRESENTED) The clock regeneration circuit according to claim 1, wherein

the bit rate detection circuit includes:

an OR gate for synthesizing the reception signal with a signal obtained by inverting the reception signal; and

a circuit for counting a change point of the output of the OR gate.

6. (CURRENTLY AMENDED) An optical signal receiver, comprising:

a light receiving element for converting a received light signal into a reception electric signal;

a PLL circuit which includes a voltage control oscillator, for synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of athe reception electric signal;

a clock extraction circuit which includes a band passing filter having a passing band width which concurrently extracts a basic waves component of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception electric signal;

a frequency detector for detecting a difference in frequencies between an output of the clock extraction circuit and an oscillation frequency of the voltage control oscillator;

a loop filter for controlling the oscillation frequency of the voltage control oscillator of the PLL circuit by a detection output of the frequency detector;

a discriminator for discriminating a level of the reception electric signal at a frequency timing of the output of the PLL circuit to output discrimination data;

a bit rate detection circuit for detecting a bit rate of the reception electric signal; and

a frequency selection circuit for outputting the oscillation frequency of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to the bit rate detected by the bit rate detection circuit, as a regeneration clock signal.

7. (CURRENTLY AMENDED) A clock regeneration circuit, comprising:

a PLL circuit including a voltage control oscillator, synchronizing an oscillation frequency signal of the voltage control oscillator with a phase of a reception signal;

a clock extraction circuit including a band passing filter having a passing band width which concurrently extracts basic wave components of the oscillation frequency signal of the voltage control oscillator and a harmonic component of a dividing signal of the oscillation frequency signal, for extracting a clock component of the reception signal; and

a frequency selection circuit outputting the oscillation frequency signal of the voltage control oscillator of the PLL circuit or a frequency signal obtained by dividing the oscillation frequency in response to a bit rate of the reception signal, as a regeneration clock signal.

8. (PREVIOUSLY PRESENTED) The clock regeneration circuit of claim 7, further comprising:

a bit rate detection circuit detecting the bit rate of the reception signal.

9. (PREVIOUSLY PRESENTED) The clock regeneration circuit of claim 8, wherein the bit rate detection circuit includes:

a first AND gate for taking a conjunction of the reception signal and the oscillation frequency signal of the voltage control oscillator of the PLL circuit;

a delay circuit for delaying an output of the first AND gate by 1 cycle of the oscillation frequency signal of the voltage control oscillator;

a second AND gate for taking a conjunction of an output of the first AND gate and an output of the delay circuit; and

a circuit for acquiring an average value of the output of the second AND gate.

10. (PREVIOUSLY PRESENTED) The clock regeneration circuit of claim 8, wherein the bit rate detection circuit includes:

an OR gate for synthesizing the reception signal with a signal obtained by inverting the reception signal; and

a circuit for acquiring an average value of the output of the OR gate.

11. (CURRENTLY AMENDED) The clock regeneration circuit according to claim 7, wherein

the clock extraction circuit further includes:

a delay circuit for delaying the reception signal by a half cycle of the ~~clock~~reception signal; and

an EX-OR circuit for acquiring an exclusive OR operation of an output of the delay circuit and the reception signal, wherein

the output of the EX-OR circuit is coupled to the band passing filter.